



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/573,017

01/19/2007

Kenji Yakushiji

Q83324

2532

23373 7590 07/21/2008  
SUGHRUE MION, PLLC  
2100 PENNSYLVANIA AVENUE, N.W.  
SUITE 800  
WASHINGTON, DC 20037

EXAMINER

CHEN, SHIZHI

ART UNIT

PAPER NUMBER

4174

MAIL DATE

DELIVERY MODE

07/21/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/573,017	<b>Applicant(s)</b> YAKUSHIJI, KENJI	
	<b>Examiner</b> SHIZHI CHEN	<b>Art Unit</b> 4174	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 6-12 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 6-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 March 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>3/22/2006 and 7/17/2008</u> . | 6) <input type="checkbox"/> Other: ____.  |

## **DETAILED ACTION**

### ***Information Disclosure Statement***

The information disclosure (IDS) submitted on 3/22/2006 and 7/17/2008 were considered by the examiner. The submission is in compliance with the provisions of 37 CFR 1.97.

### **Priority**

Certified Copy of Foreign Priority Application submitted under 35 U.S.C. 119(a)-(d) was considered by the examiner.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3 and 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. (Patent Number: 6,156,584; hereinafter Itoh) in view of Bruhns et al. (Pub. No.: US 2004/0051118 A1; hereinafter Bruhns).

Regarding claims 1 and 12, Itoh teaches a method for the fabrication of a semiconductor light-emitting device, comprising the steps of:

stacking at least a first conductive type semiconductor layer (3 in Fig. 2; Col. 3 Line 50, “n-type layer 3”), an active layer (4 in Fig. 2; Col. 3 Line 53, “active layer 4”) and a second conductive type semiconductor layer (5 in Fig. 2; Col. 3 Lines 50-51, “p-type layer (clad layer) 5”) on a substrate (1 in Fig. 2; Col. 3 Line 46, “substrate 1 of sapphire”) to form a wafer;

forming on a side of growth surfaces of the semiconductor layers (3/4/5 in Fig. 2) first trenches (the rectangular trench along S line in Fig. 2) exposing the first conductive type semiconductor layer (3);

forming second trenches (1b in Fig. 2) reaching the substrate (1) from above the first trenches (the rectangular trench along S line);

forming third trenches (1a in Fig. 2) from the substrate (1) at positions corresponding to the second trenches (1b);

using a dicing blade (Col. 1 Lines 33-35, “the resultant structure is scribed at boundary portions S between chips with a diamond scriber or the like, forming notches 21a”) to correct a shape of the third trenches (1a); and dividing the wafer into chips.

However, Itoh fails to teach forming the second and third trenches by the use of a laser beam.

Bruhns teaches the trench can be formed by the use of a laser beam (Paragraph [0040] line 5, “the trench is formed by sawing or laser scribing”).

It would have been obvious for the person with ordinary skill in the art at the time the invention was made to modify Itoh’s teaching with suggestions of Bruhns by forming

the second and third trenches using a laser beam for the purpose of etching through the sapphire substrate efficiently.

Regarding claims 2 and 3, Itoh and Bruhns disclose the claimed invention except that the third trenches have a greater width than the first and second trenches. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the third trench with width greater than the first and second trenches, since the difference in the width of the trenches will not support the patentability of the subject matter encompassed by the prior art unless there is evidence indicating such width are critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d (Fed.cir), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

Regarding claim 6, Itoh and Bruhns disclose the claimed invention except that the third trenches are formed by radiating a laser beam two times or more. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the third trenches by radiating a laser beam two times or more, since the difference in how many times a laser is radiated will not support the patentability of the subject matter encompassed by the prior art unless there is evidence indicating such number of times a laser is radiated are critical. "[W]here the general conditions of a

claim are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation.” See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d (Fed.cir), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

Regarding claim 7, Itoh teaches the substrate (1 in Fig. 2) is lapped, ground or polished (Col. 1 Lines 49-51, “locally etching the semiconductor layer laminate to make it thinner and forming notches at the back of the substrate before chip separation”) till a thickness inclusive of an epitaxial layer (3/4/5 in Fig. 2) prior to the formation of the third trenches (1a in Fig. 2).

However, Itoh fails to teach the thickness of the substrate inclusive of an epitaxial layer reaches 100 um or less.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to polish the substrate to a thickness which reaches 100 um or less inclusive an epitaxial layer prior to the formation of the third trenches, since the difference in the thickness will not support the patentability of the subject matter encompassed by the prior art unless there is evidence indicating such thickness are critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation.” See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406

F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d (Fed.cir), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

Regarding claim 8, Itoh teaches the first conductive type semiconductor layer (3 in Fig. 2; Col. 3 Line 50, “n-type layer 3”) is an n-type semiconductor layer and the second conductive type semiconductor layer (5 in Fig. 2; Col. 3 Lines 50-51, “p-type layer (clad layer) 5”) is a p-type semiconductor layer.

Regarding claim 9, Itoh teaches the substrate (1 in Fig. 2; Col. 3 Line 46, “substrate 1 of sapphire”) is a sapphire substrate.

Regarding claims 10 and 11, Itoh teaches the semiconductor light-emitting device (11/12 in Fig. 2; Col. 3 Line 26, “a plurality of LED chips 11,12”) is a gallium nitride-based semiconductor (Col. 3 Lines 50-52, “the p-type layer (clad layer) 5, which is comprised of a p-type AlGaIn-based compound semiconductor layer and/or GaN layer”) light-emitting device.

### **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHIZHI CHEN whose telephone number is (571)270-5376. The examiner can normally be reached on Monday - Friday (ALT) 7:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nguyen D. Kimberly can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. C./  
Examiner, Art Unit 4174

/Kimberly D Nguyen/  
Supervisory Patent Examiner, Art Unit 4174